

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO PROCESSOR SYSTEM

- (71) We, STANDARD TELE-
 PHONES AND CABLES LIMITED, a
 British Company of 190 Strand, London
 W.C.2. England, do hereby declare the
 invention, for which we pray that a patent
 may be granted to us, and the method by
 which it is to be performed, to be particular-
 ly described in and by the following state-
 ment:
 10 This invention relates to a multi-processor
 system of the type in which a so-called
 executive processor controls a set of so-
 called slave computers each of which is
 allotted a programme for it to execute.
 15 In such a system it is necessary for the
 executive processor to be aware of the
 serviceability conditions of the slave proces-
 sors which it controls. Information as to
 these conditions may be obtained partly
 20 from the results of the tasks allotted to the
 slave computers and partly from routining,
 but not all failures of the slave processors
 are rapidly and readily discernible by the
 executive processor from the effects of
 25 failures.
 An object of the present invention is to
 assist the executive processor's rapid deter-
 mination of a large part of the possible
 malfunctions of the slave processors.
 30 According to the present invention there
 is provided a multi-processor system which
 includes an executive digital processor and a
 plurality of slave digital processors, in which
 data processing tasks are allotted to the
 35 slave processors by the executive processor
 for the slave processors to execute those
 tasks, in which during the execution of a
 said task a sequence of summation opera-
 tions is performed on words read from a
 40 memory which contains the programme for
 the slave processor executing that task, and
 in which the results of said sequence sum-
 mation operations are checked by the ex-
 ecutive processor at predetermined inter-
 45 vals, the correctness or otherwise of the

operations of the slave processor being
 assessed on the basis of the results of said
 checks.

An embodiment of the invention will now
 be described with reference to the highly
 schematic block schematic drawing accom-
 panying the Provisional Specification.

In the arrangement described herein, the
 slave processors perform their functions in a
 simple cyclic manner, and each of the slave
 processors acts as a major part of a signall-
 ing terminal in a multi-exchange telecom-
 munication system. The programme cycles
 around a closed loop of instructions, the
 loop having branchings which are followed
 or not, dependent on the conditions found
 on the signalling highway or highways under
 control. The operational conditions of the
 signalling terminal may also influence the
 manner in which the program cycles.

In every cycle of the programme a differ-
 ent control word for the programme for the
 slave processor 1 is read from the read only
 memory programme store 2 and is added to
 the contents of a pair of sum registers. Each
 such word is a 16 bit, i.e. two byte, word and
 the upper and lower bytes of this word are
 added respectively to different ones of the
 sum registers. In the execution of these
 additions each upper byte is shifted to the
 lower byte position before it is added to its
 sum register.

The two sum registers are set to zero at
 the beginning of the scan of all of the control
 words in the store such as 2 which contains
 the programme and its associated fixed
 data. The address of the word read from the
 read-only store 2 which is read, split into its
 bytes, and added to the sum registers is
 incremented by one after each such addi-
 tion. This procedure continues until the
 contents of the last word location of the
 store 2 have been accessed and added to the
 sum registers.

When the last word has been read and

added to the sum registers, the contents of those sum registers are transferred to two results registers in a storage area 3 which is a random access memory usable either by the slave processor 1 or the executive processor (not shown). This storage area 3 is accessible for either read or write via selectors 4, 5, as required.

The "worst case" acceptable time taken to complete one of these sum check sequences on the memory 2 by the slave processor 1 is known, and the executive processor accesses the results register in the storage area 3 at intervals greater than the above-mentioned worst case time.

If the contents of the results registers when thus checked by the executive processor are not as expected then that slave processor is not functioning correctly and the executive processor takes the necessary action. This could be the disablement of the failed slave processor, plus the transfer of its tasks to a different processor or processors, plus the giving of an alarm to the maintenance staff.

If the results are correct on the above check, the executive processor resets the results registers to zero, and then checks to see if the resetting has in fact been correctly performed.

In an example described above the executive processor checks each slave processor's results registers once per second.

WHAT WE CLAIM IS:

1. A multi-processor system which includes an executive digital processor and a plurality of slave digital processors, in which data processing tasks are allotted to the slave processors by the executive processor for the slave processors to execute those tasks, in which during the execution of a said task a sequence of summation operations is performed on words read from a memory which contains the programme for the slave processor executing that task, and in which the results of said sequence of summation operations are checked by the executive processor at predetermined intervals, the correctness or otherwise of the operations of the slave processor being assessed on the basis of the results of said checks.

2. A system as claimed in claim 1, in which each said slave processor executes the task allotted to it in a cyclic manner by the execution of a closed loop of instructions, with or without branchings, and in which on each cycle of the loop a control word for the slave processor is read from a read-only memory, said sequence of summation operations being effected on said control words.

3. A system as claimed in claim 2, in which each said control word is split into an upper portion and a lower portion for said summation, in which the upper portions of

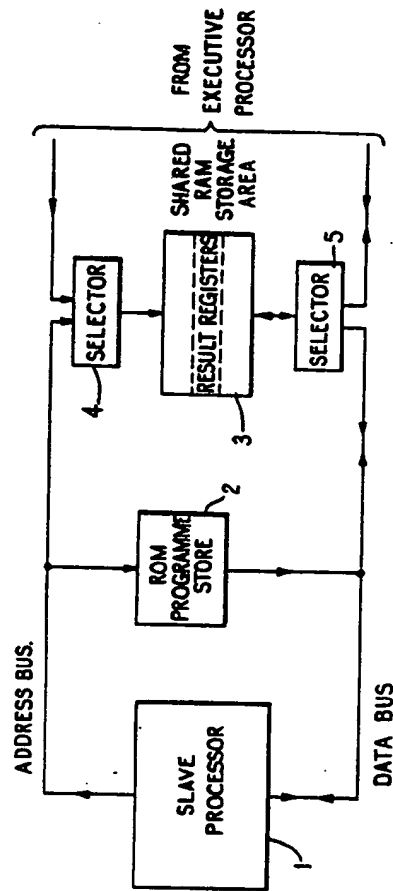
successive ones of said control words are summated in a first sum register and the lower portions of successive ones of said control words are summated in a second sum register, in which the two sums thus produced are transferred respectively to first and second result registers, in which the time taken for a complete summation sequence of control words in one of said slave processors is known, and in which remedial action is taken in respect of a slave processor if the said time exceeds a pre-set maximum acceptable value.

4. A multi-processor system substantially as described with reference to the drawing accompanying the provisional specification. Reference has been directed in pursuance of section 9, subsection (1) of the Patents Act 1949, to patent No. 1324250

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